CONTINUOUS INTERNAL EVALUATION- 1

Dept: **CSE**	Sem / Div: **4CS A & B**	Sub: **Microcontroller & Embedded Systems**	S Code: **18CS44**
Date: 25.05.2021	Time: 3:00-4:30	Max Marks: 50	Elective: N
Note: Answer any 2 full questions, choosing one full question from each part.			

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QN		Questions	Marks	RBT	COs
		PART A			
1	a	Explain ARM core data flow model with neat diagram.	9	L2	CO1
	b	List and explain seven ARM processor modes. Also, explain ARM core changing from user mode to interrupt request mode on an exception, with a neat diagram	9	L2	CO1
	c	Differentiate: Microprocessors vs Microcontrollers.	7	L3	CO1
		OR			
2	a	What is pipeline? Compare ARM7 three-stage pipeline, ARM9 five-stage pipeline, and ARM10 six-stage pipeline.	9	L2	CO1
	b	Explain Exception or Interrupt. Narrate Interrupt Vector Table.	9	L2	CO1
	c	Discuss hardware extensions for ARM core.	7	L3	CO1
		PART B			
3	a	Explain single-register load-store addressing modes with examples.	9	L3	CO2
	b	Explain program status register instructions. Also, Write a code fragment to – (i) Copy the cpsr into register r1 (ii) Clear bit 7 of r1 (iii) Copy the register r1 back to cpsr	9	L3	CO2
	c	Explain the following ARM Instructions with examples: A) BIC B) STMIB C) MRS D) LDMIA E) SWP F) LDR G) MUL	7	L2	CO2
		OR			
4	a	With neat diagram and example, explain block memory transfer in the memory map using load-store multiple instructions.	9	L3	CO2
	b	Explain stack operation of ARM processors. Also explain the load-store multiple addressing aliases available to support stack operations.	9	L3	CO2
	c	Explain software interrupt instruction with an example.	7	L2	CO2